RENAMING FOR REGISTER WITH MULTIPLE BIT FIELDS

Abstract of the Invention

[000103] An apparatus and method are provided for renaming a logical register for which bit accesses of varying lengths are permitted, such as a predicate register. Rename logic supports renaming for both partial-bit accesses and bulk-bit accesses to bits of the register. Rename logic utilizes a rename map table associated with the logical register to be renamed and also includes a plurality of physical rename registers. They physical rename registers include a set of skinny physical rename registers to be used for renaming for partial-bit writes. The physical rename registers also include a set of fat physical rename registers to be used for renaming for bulk-bit writes. Additional sizes of physical rename registers may also be employed. The entries of the single physical rename map table may point to either fat or skinny physical rename registers.